REMARKS

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 2-8, 12-13 and 16 are pending in this application. No claims are amended herein. No claims have been allowed.

Claim Rejections - 35 U.S.C. § 103

1. The Examiner has rejected claims 3-7, 12-13 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Kelly et al. (U.S. Patent No. 6,143,117; hereinafter "Kelly") in view of Mountain (U.S. Patent No. 6,013,534) and Haq (U.S. Patent No. 6,245,677).

Applicant notes that the Examiner acknowledges at page 3, first full paragraph of the office action made FINAL that Kelly fails to disclose removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer, in accord with applicant's invention as disclosed and claimed within claim 16.

Rather the Examiner relies therein upon Mountain at Figs. 10-11 for a disclosure of removing a substrate while employing a dielectric layer as a stop layer. The Examiner also appears to extend Mountain to provide for removing a substrate while employing a dielectric isolated metallization pattern of Kelly as a stop layer since the Examiner asserts that the same is a conventional process that may be employed to reduce thicknesses and provide better handling of microelectronic fabrications, as disclosed within Mountain.

Further, the Examiner within the paragraph bridging pages 3-4 of the office action made FINAL relies upon Haq for a disclosure of a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods for removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication.

In response in a first instance, while applicant notes that the Examiner has accurately cited Mountain as disclosing removing a substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric layer (or alternatively a metal layer) as a stop layer, applicant asserts that Mountain neither explicitly nor implicitly discloses removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer. Applicant further notes that the Examiner does not apparently assert that Mountain explicitly discloses the same. Applicant yet further notes that within the context of Mountain's invention Mountain's etch stop layer is an extrinsic etch stop layer employed only for etch stop purposes. Thus, Mountain implicitly would have no motivation to employ a dielectric isolated metallization pattern for etch stop purposes, but rather an etch stop layer formed of a single etch stop material appears entirely adequate within Mountain's invention. Thus, applicant asserts that Mountain neither explicitly nor implicitly discloses a dielectric isolated metallization pattern as a stop layer when removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication.

With respect to the Examiner's assertion of suggestion or motivation for modification or combination of Mountain with Kelly predicated upon reduction of thickness of a microelectronic fabrication such as to provide better handling thereof, applicant notes that Mountain at col. 1, lines 36-47 discloses that thicker semiconductor substrates, rather than thinner semiconductor substrates, provide for better handling (i.e., less breakage) of semiconductor fabrications, inapposite to that which is asserted by the Examiner.

In accord with the above, applicant first asserts that each and every limitation within applicant's invention as disclosed and claimed within claim 16 is neither explicitly nor implicitly disclosed within Kelly or Mountain, in particular with respect to removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer. In addition, applicant second asserts that there exists no suggestion or motivation for modification or combination of Kelly with Mountain for reasons as cited by the Examiner, since Mountain teaches away from the reasons as cited by the Examiner.

In response in a second instance, applicant next notes that while Haq, as cited by the Examiner, does disclose a polishing method for backside thinning of a substrate, such as a semiconductor substrate, Haq does not apparently require a dielectric isolated metallization pattern be formed upon Haq's substrate prior to thinning thereof, nor does Haq disclose employing the dielectric isolated metallization pattern as a stop layer when thinning Haq's substrate. Applicant further notes that Haq's invention is preferably employed with the context of a semiconductor substrate having defined on the front side thereof live circuits that presumably may include a dielectric isolated metallization pattern such as to access semiconductor devices employed within the live circuits and formed within the semiconductor

substrate (col. 3, lines 18-24). Under such circumstances where a semiconductor substrate having formed therein semiconductor devices and formed thereupon a dielectric isolated metallization pattern to access the semiconductor devices and live circuits formed therefrom is completely thinned and removed while employing the dielectric isolated metallization pattern as a stop layer, Haq's invention is rendered inoperative for its intended purpose since such complete thinning and removal of Haq's semiconductor substrate would also remove Haq's semiconductor devices and render inoperative Haq's live circuits. Thus, in addition to not unambiguously providing each and every limitation within applicant's invention as disclosed and claimed within claim 16 with respect to removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer, Haq if extended to provide limitations in accord with applicant's claimed invention may not properly be combined with Kelly and Mountain to reject any of applicant's claims to applicant's invention, since Haq is rendered inoperative upon such extension. MPEP 2143, 2143.01. Applicant finally notes that Haq apparently also teaches away from applicant's claim 12 and for that reason also may not properly be employed in rejecting any of applicant's claims to applicant's invention. MPEP 2141, 2141.02.

Thus, since: (1) the Examiner acknowledges that Kelly does not disclose removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer; (2) applicant asserts (as not apparently expressly contradicted by the Examiner) that Mountain does not expressly or implicitly disclose removing a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer; (3) there exists no suggestion or motivation for modification or combination or Kelly with Mountain for reasons as cited by the

Examiner; and (4) Haq if extended to provide for removal of a second substrate from a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication while employing a dielectric isolated metallization pattern as a stop layer is rendered inoperative for Haq's intended purposes, applicant asserts that at minimum each and every limitation within applicant's invention as disclosed and claimed within claim 16 is not disclosed within Kelly, Mountain, Haq or any combination thereof and thus at minimum claim 16 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq. Since at minimum all remaining claims within the foregoing rejection are dependent upon claim 16 and carry all of the limitations of claim 16, applicant additionally asserts at minimum that those remaining claims may also not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejections of claims 3-7, 12-13 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq be withdrawn,

2. The Examiner has rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Davidson (U.S. Patent No. 5,880,010).

3. The Examiner has rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Kresge et al. (U.S. Patent No. 6,066,808; hereinafter "Kresge").

While not precluding the existence of independent patentable distinctions between:: (1) Kelly in view of Mountain and Haq: and (a) Davidson; or (b) Kresge; and (2) that which is claimed within claim 2 and claim 8, applicant predicates patentability of claim 2 and claim 8 upon their dependence upon claim 16.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejections of: (1) claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Davidson; and (2) claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Kelly in view of Mountain and Haq, and further in view of Kresge, be withdrawn.

Response to Arguments

Within the second full paragraph on page 7 of the office action made FINAL, and in response to the Examiner's assertion that Haq was relied upon for thinning of semiconductor substrates when employing chemical mechanical polish (CMP) planarizing methods, applicant notes that an Examiner is required to consider a prior art reference in its entirety, including portions thereof that teach away from an applicant's claimed invention. MPEP 2141, 2141.02.

Within the paragraph bridging pages 7-8 of the office action made FINAL and in response to the Examiner's assertion that applicant's etch stop layer does not comprise a dielectric isolated metallization pattern but rather applicant's dielectric isolated metallization pattern comprises an etch stop layer, applicant notes that applicant is permitted to be applicant's own lexicographer and that applicant's claimed invention is otherwise clear within the context of applicant's disclosure. MPEP 2173, 2173.01, 2173.02.

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Other Considerations

The Examiner has cited no additional prior art of record not employed in rejecting applicant's claims to applicant's invention. No fee is due as a result of this response.

SUMMARY

Applicant's invention as disclosed and claimed within claim 16 provides a laminating method for forming a microelectronic fabrication. The laminating method laminates a partially fabricated semiconductor integrated circuit microelectronic fabrication with a dielectric isolated metallization pattern formed in inverted order over a second substrate. The second substrate is then removed employing a removal method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing methods, and while employing the dielectric isolated metallization pattern as a stop layer. At minimum absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention as disclosed and claimed within claim 16.

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested. Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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